PCE04I Inmarsat Turbo Encoder

11 October 2024 (Version 1.01) Product Specification

PCE04I Features

- 16 state Inmarsat compatible turbo encoder
- Rate 1/2 to 1/5
- Data lengths from 8 to 32,764 bits
- Up to 1145 MHz internal clock
- Up to 572 Mbit/s encoding speed
- Parallel encoded data out
- 118 6–input LUTs
- Available as EDIF and VHDL core for Xilinx FPGAs under SignOnce IP License. ASIC, Intel/Altera, Lattice and Microsemi/Actel cores available on request.

Introduction

The PCE04I is a 16 state Inmarsat [1,2] compatible turbo encoder. Data lengths from 8 to 32,764 bits can be implemented. Turbo code rates from 1/2 to 1/5 can be selected. The sequential data is terminated with a tail. The data and this tail are interleaved. The input data block size is *K*. The interleaver size is *K*+4. The number of coded bits is *n*(*K*+4) where the nominal code rate is 1/*n*.

Figure 1 shows the schematic symbol for the PCE04I encoder. The EDIF core can be used with Xilinx Foundation or Integrated Software Environment (ISE) software. The VHDL core can be used with Xilinx ISE or Vivado software. Custom VHDL cores can be used in ASIC designs.

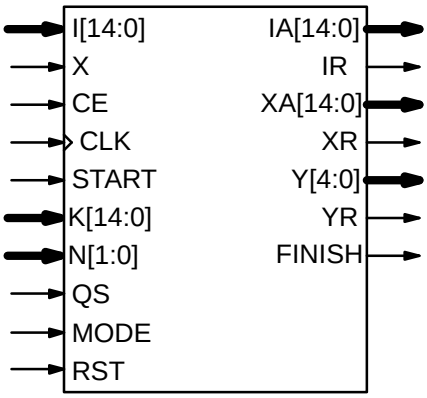

Figure 1: PCE04I schematic symbol.

Table 1 shows the performance achieved for various Xilinx parts for K = 32,764. T_{cp} is the minimum clock period over recommended operating conditions. These performance figures may change due to device utilisation and configuration.

Note that Zynq devices up to XC7Z020 and from XC7Z030 use programmable logic equivalent to Artix–7 and Kintex–7 devices, respectively.

Table 1: Example performance

Part	T_{cp} (ns)	Speed (Mbit/s)	
		QS = 0	QS = 1
XC7S6–1	3.204	104.0	156.0
XC7S6–2	2.595	128.4	192.6
XC7A12T–1	3.312	100.6	150.9
XC7A12T–2	2.730	122.0	183.1
XC7A12T–3	2.432	137.0	205.5
XC7K70T–1	2.100	158.7	238.0
XC7K70T–2	1.717	194.1	291.1
XC7K70T–3	1.628	204.7	307.0
XCKU035–1	1.847	180.4	270.6
XCKU035–2	1.524	218.6	328.0
XCKU035–3	1.339	248.9	373.3
XCKU3P–1	1.156	288.3	432.4
XCKU3P–2	0.989	336.9	505.4
XCKU3P–3	0.873	381.7	572.6

Signal Descriptions

CE	Clock Enable
CLK	Encoder Clock
FINISH	Encoder Finish
I	Interleaver Address Input
IA	Interleaver Address ROM Address
IR	Interleaver Address ROM Ready
K	Data Length (8 to 32,764)
MODE	0 = small interleaver (XA[14:13] = 0)
	1 = large interleaver
N	2 = Rate 1/2
	3 = Rate 1/3
	0 = Rate 1/4
	1 = Rate 1/5
QS	Second Parity Select
	0 = Second encoded output is X, P and Q
	1 = Second encoded output is Q
RST	Synchronous Reset
START	Encoder Start
X	Data In
XA	Data In Address
XR	Data In Ready

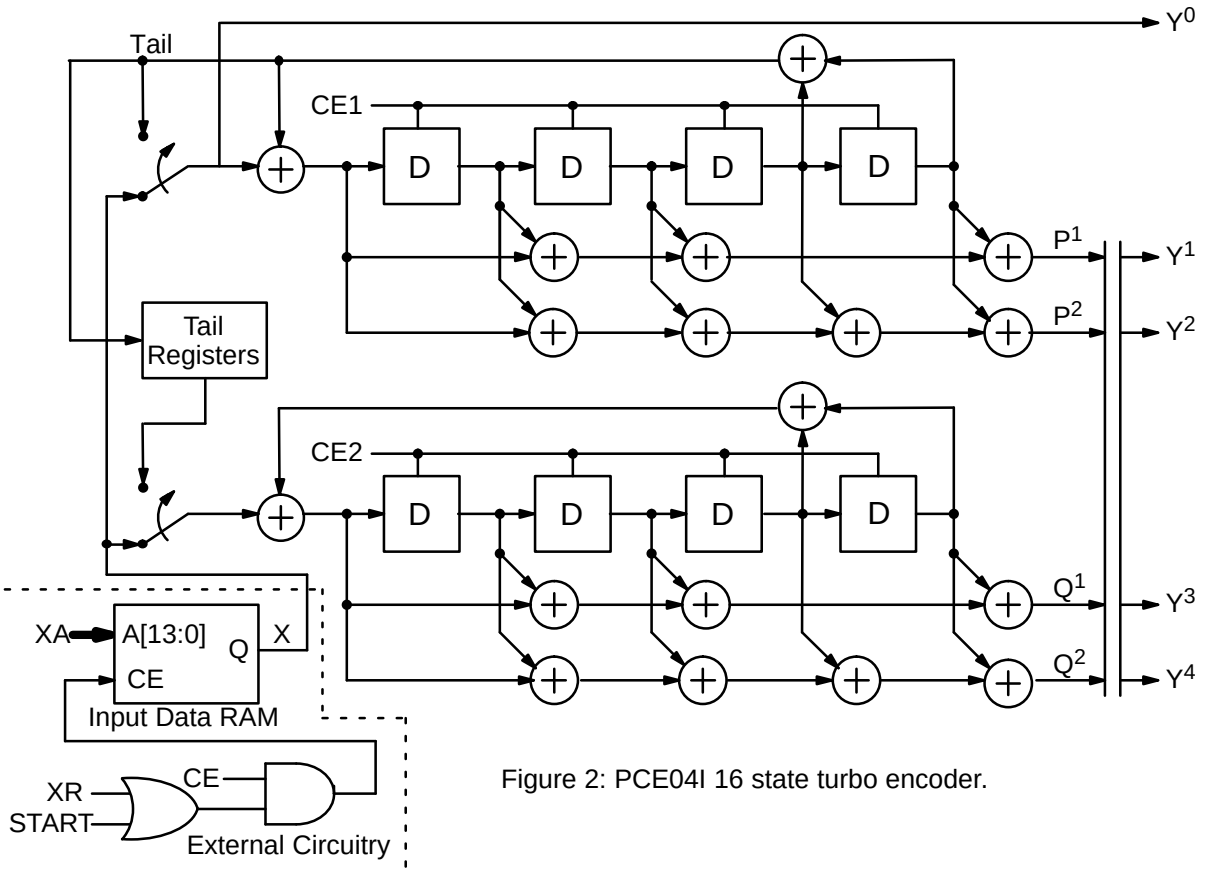

Figure 2: PCE04I 16 state turbo encoder.

Y	Data Out
YR	Data Out Read

Encoder

Figure 2 gives a block diagram of the PCE04I Inmarsat 16 state turbo encoder. X is the data input and Y0 to Y4 are the coded outputs. Data is clocked during the low to high transition of CLK. Separate internal clock enables (CE1 and CE2) are used to clock the data into each encoder. Non–interleaved data is clocked into the first encoder and interleaved data is clocked into the second encoder. The vertical lines indicate multiplexers

The data is first input in the sequence X_k, from $k = 0$ to K–1. The encoder then forms the tail bits from $k = K$ to K+3 which are stored in the tail registers. Encoded data is also output, with $Y_k^0 = X_k$, $Y_k^1 = P_k^1$ and $Y_k^2 = P_k^2$, regardless of the value of N[1:0].

If QS = 0, the data is then input in the sequence $X_k\ X_{I(k)}$ from $k = 0$ to K–3 where $I(k)$ is the interleaved address. Table 2 shows the output sequence for the various code rates. For rate 1/3 and 1/5, k is incremented by one from 0 to K–3. For rate 1/2 and 1/4, k is incremented by two.

If QS = 1, data is then input in the interleaved sequence $X_{I(k)}$ from $k = 0$ to K–3. The encoded output is $Y_k^0 = X_{I(k)}$, $Y_k^1 = Q_k^1$ and $Y_k^2 = Q_k^2$, regardless of the value of N[1:0].

Table 2: Output sequence (QS = 0)

Rate	Sequence
1/2	$Y^0 = X_k\ X_{k+1}$
	$Y^1 = P_k^1\ Q_{k+1}^1$
1/3	$Y^0 = X_k$
	$Y^1 = P_k^1$
	$Y^2 = Q_k^1$
1/4	$Y^0 = X_k\ X_{k+1}$
	$Y^1 = P_k^1\ P_{k+1}^1$
	$Y^2 = P_k^2\ Q_{k+1}^1$
	$Y^3 = Q_k^2\ Q_{k+1}^2$
1/5	$Y^0 = X_k$
	$Y^1 = P_k^1$
	$Y^2 = P_k^2$
	$Y^3 = Q_k^1$
	$Y^4 = Q_k^2$

Figure 3 shows the initial timing diagram for encoding a block of data of length K = 1232. The encoder starts and ends in state 0. When the encoder requires data X to be read from the input RAM, the data ready signal XR goes high (except for the first symbol) and XA[14:0] selects the data bit.

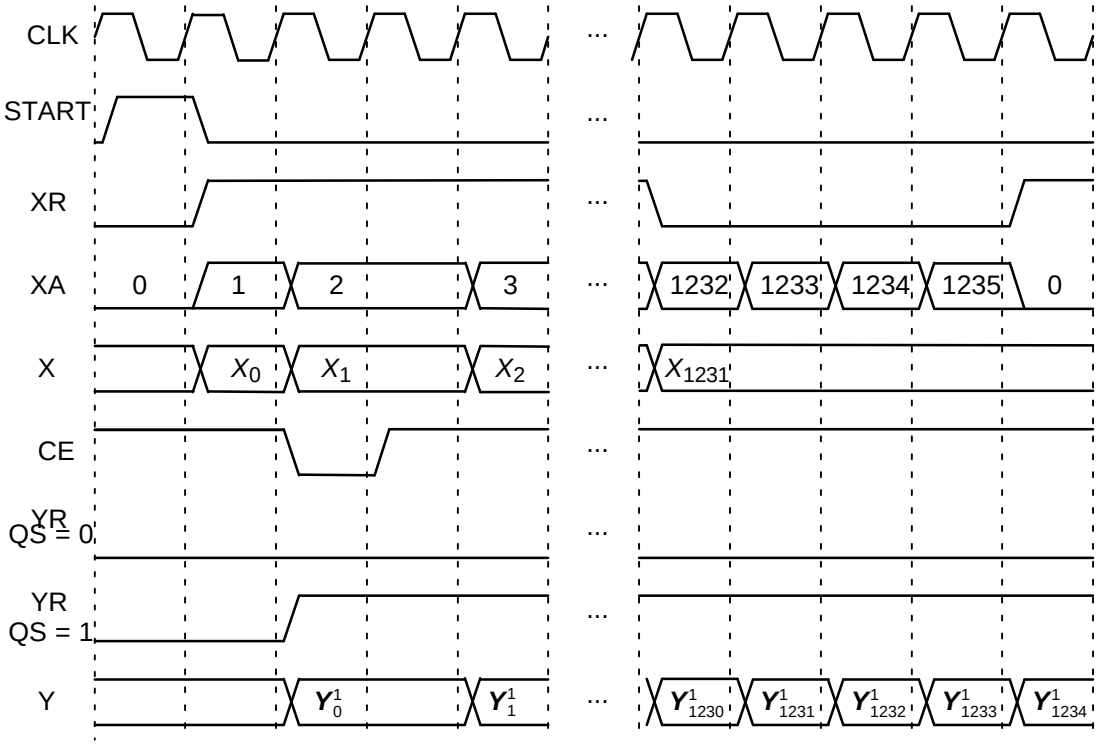

Figure 3: PCE04I Initial Encoder Timing (K = 1232).

After a START signal is initiated XR goes high after one clock cycle. All signals are held if CE goes low. It is assumed that the data is stored in a synchronous read RAM with (START OR XR) AND CE used to control the read enable input of the RAM. An asynchronous read RAM can also be used by registering the RAM output. For QS = 1, the encoded data ready signal YR goes high two clock cycles after a START signal is initiated. YR is high for both the data block and tail. For QS = 0, YR stays low until the second encoded output.

Figures 4 and 5 shows the second block encoding for QS = 0 and 1, respectively. Symbol $\boldsymbol{Y}^1_k$ represents outputs with $Y^0_k = X_k$, $Y^1_k = P^1_k$ and $Y^2_k = P^2_k$. Symbol $\boldsymbol{Y}^2_k$ represents outputs with $Y^0_k = X_{I(k)}$, $Y^1_k = Q^1_k$ and $Y^2_k = Q^2_k$,. Symbol $\boldsymbol{Y}_k$ represents the outputs given in Table 2.

For QS = 0, the nominal encoder speed f_e is

$$f_e = \frac{f_E}{3 + 15/K} \tag{1}$$

where $f_E = 1/T_{cp}$ is the encoder clock speed. For QS = 1 the encoder speed is

$$f_e = \frac{f_E}{2 + 8/K}. \tag{2}$$

Ordering Information

SW–PCE04I–SOP (SignOnce Project License)
SW–PCE04I–SOS (SignOnce Site License)
SW–PCE04I–VHD (VHDL ASIC License)

All licenses include Xilinx EDIF and VHDL cores. The SignOnce Project (SOP) license allows unlimited instantiations for a specified project. The SignOnce Site (SOS) license allows unlimited instantiations and projects for a specified development site. The EDIF core can be used for Virtex–2, Spartan–3 and Virtex–4 with Foundation or ISE software. The VHDL core can be used for Virtex–5, Spartan–6, Virtex–6, 7–Series, UltraScale and UltraScale+ with ISE or Vivado software.

Note that *Small World Communications* only provides software and does not provide the actual devices themselves. Please contact *Small World Communications* for a quote.

References

[1] University of South Australia, “Reduced bandwidth study of the High Speed Data Service Final Report,” SCRC96–6532–D005, Sep. 1996.

[2] Xu Youyun, Luo Hanwen, Song Wentao, “Application of TC in the Inmarsat mobile satellite communication systems,” Mobile Communication, 1999, 3rd.

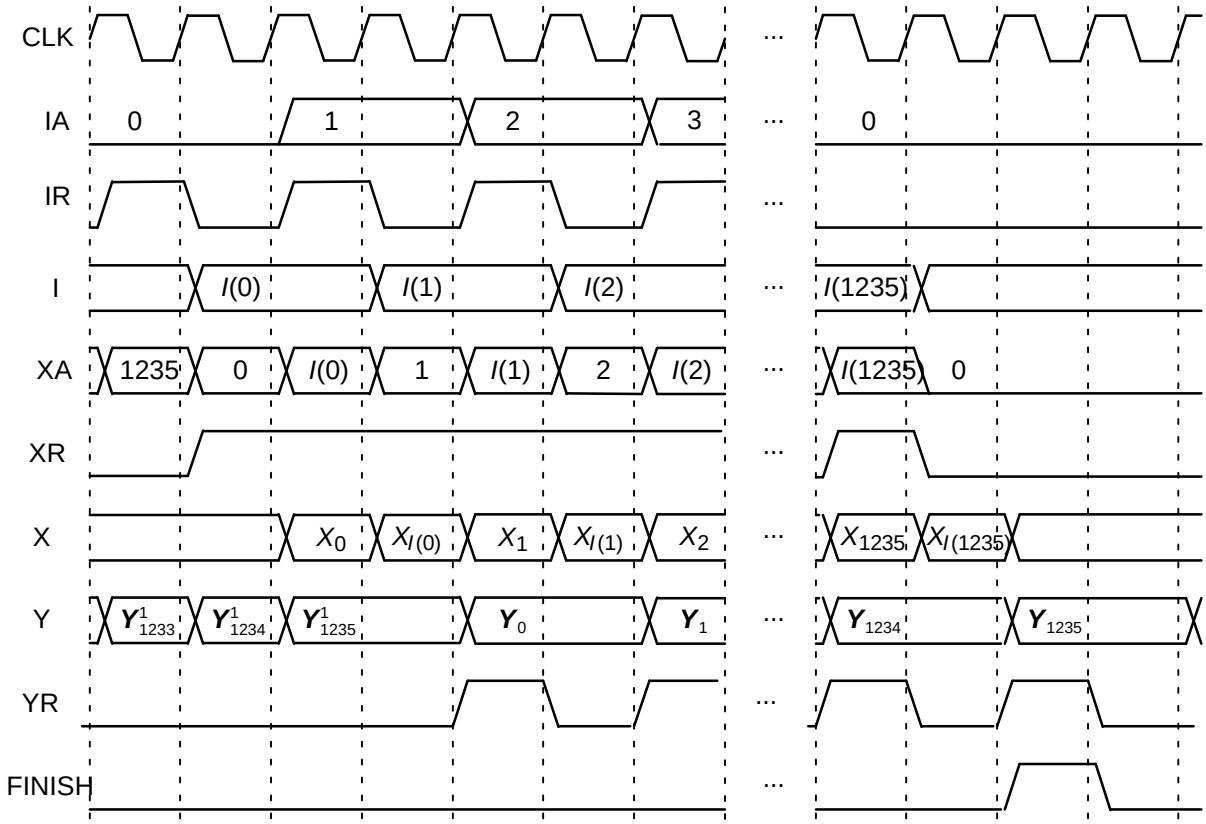

Figure 4: PCE04I Second Encoder Timing (*K* = 1232, QS = 0, CE = 1).

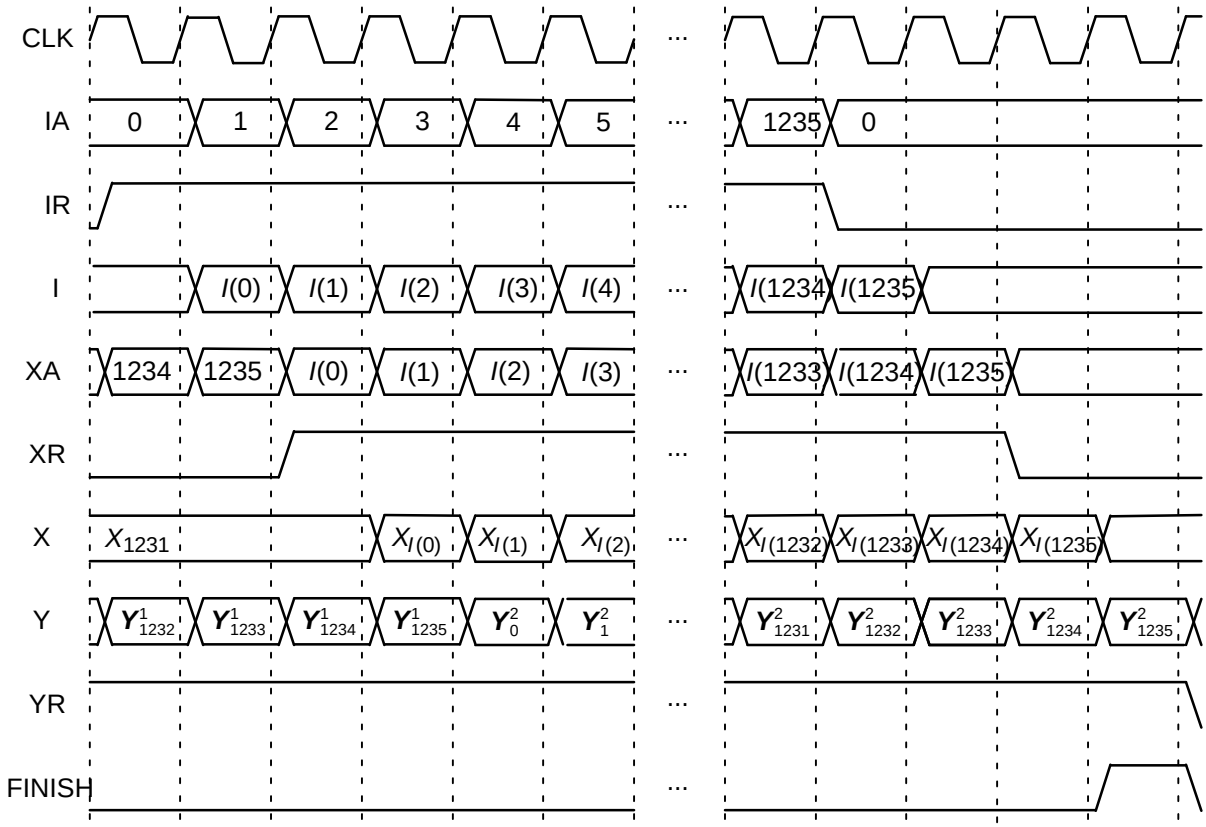

Figure 5: PCE04I Second Encoder Timing (*K* = 1232, QS = 1, CE = 1).

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Version History

- 0.00 28 September 2014. Preliminary product specification.
- 0.01 3 October 2014. Corrected schematic symbol and encoder diagram.
- 1.00 2 November 2014. Added LUT complexity and example performance values. Added FINISH output to encoder symbol and timing diagrams. Corrected Table 2.
- 1.01 11 October 2024. Updated LUT complexity. Deleted Spartan–6, Virtex–5, Virtex–6 and Zynq–7 performance. Updated Artix–7 and Kintex–7 performance. Added Spartan–7, Kintex UltraScale and Kintex UltraScale+ performance.