PCE03L Features

- 8 state 3GPP™ LTE compatible turbo encoder
- Rate 1/3
- 40 to 6144 bit interleaver
- Up to 302 Mbit/s encoding speed
- Parallel encoded data out
- 218 slices for Virtex–II, Spartan–3 and Virtex–4. 240 LUTs for Virtex–5, Virtex–6 and Spartan–6.
- Available as EDIF core and VHDL simulation core for Xilinx FPGAs under SignOnce IP License. Actel, Altera and Lattice FPGA cores available on request.
- Available as VHDL core for ASICs
- Low cost university license also available

Introduction

The PCE03L is an 8 state 3GPP™ LTE [1] compatible turbo encoder. Encoded data is output in parallel for increased speed. The LTE turbo code uses two 8 state systematic recursive convolutional code. The interleaver uses a simple quadratic permutation interleaver.

For 3GPP™ LTE, there are 188 interleaver sizes ranging from 40 to 6144 bits. Two parameters f_1 and f_2 are used by the interleaver. All interleaver sizes from 40 to 504 bits that are a multiple of 8, 512 to 1008 bits that are a multiple of 16, 1024 to 2016 bits that are multiple of 32, and 2048 to 6144 bits that are a multiple of 64 are specified.

For 3GPP™, each tail of the two constituent encoders are terminated using all the data and parity bits (for a total of 12 bits for rate 1/3).

Figure 1 shows the schematic symbol for the PCE03L encoder. The EDIF core can be used with Xilinx Integrated Software Environment (ISE) software to implement the core in Xilinx FPGA's. The VHDL core can be used in ASIC designs.

Table 1 shows the performance achieved with 3GPP™ LTE for various Xilinx parts and K = 6144. T_{cp} is the minimum clock period over recommended operating conditions. These performance figures may change due to device utilisation and configuration.

Only one global clock is used. No other resources are used except for external input memory.

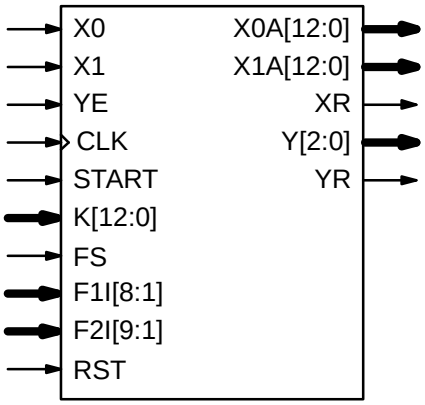

Figure 1: PCE03L schematic symbol.

Table 1: Example performance

Part	T_{cp} (ns)	Speed (Mbit/s)
XC3S50A–4	10.568	94.5
XC3S50A–5	8.813	113.3
XC6SLX4–2	8.808	113.4
XC6SLX4–3	6.775	147.4
XC4VFX12–10	6.945	143.8
XC4VFX12–11	5.922	168.7
XC4VFX12–12	5.264	189.8
XC5VLX30–1	5.154	193.8
XC5VLX30–2	4.419	226.0
XC5VLX30–3	3.928	254.3
XC6VLX75T–1	4.315	231.5
XC6VLX75T–2	3.722	268.4
XC6VLX75T–3	3.302	302.5

Signal Descriptions

CLK	Clock
F1I	LTE external parameter 1 (0 to 255) F1I = f_1 div 2.
F2I	LTE external parameter 2 (0 to 511) F2I = f_2 div 2.
FS	LTE external parameter select 0 = Select internal parameters 1 = Select external parameters
K	Interleaver Length (40–6144)
RST	Synchronous Reset
START	Encoder Start
X0	Non–interleaved Data In

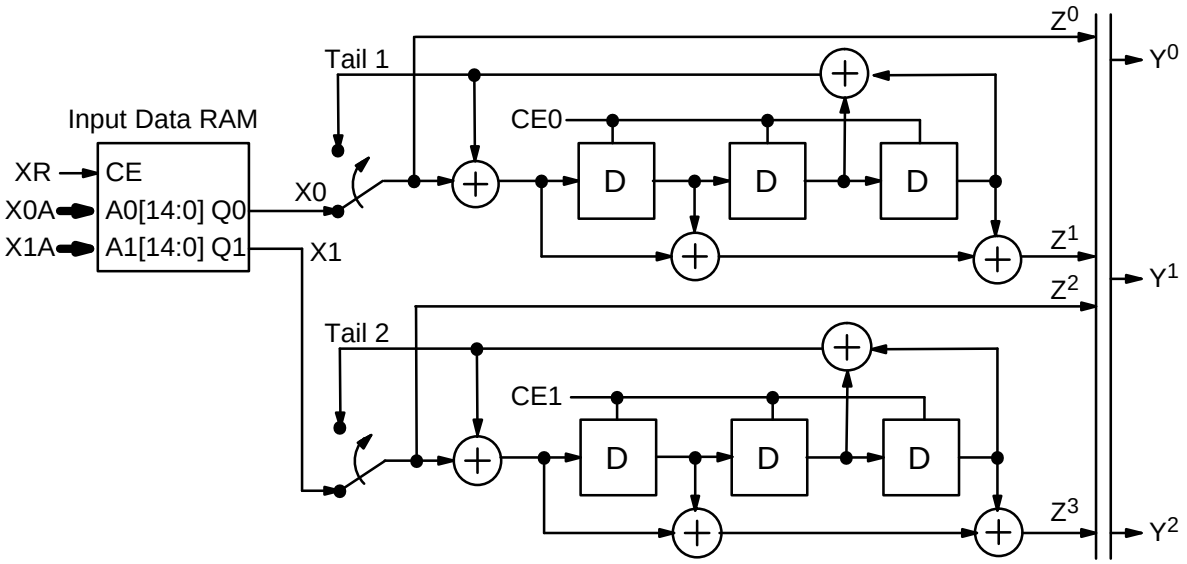

Figure 2: PCE03L eight state turbo encoder.

X1	Interleaved Data In
X0A	Non–interleaved Data In Address
X1A	Interleaved Data In Address
XR	Data In Ready
Y	Encoded Data Out (data and parity)
YE	Encoded Data Out Enable
YR	Data Out Ready

Encoder

Figure 2 gives a block diagram of the PCE03L 3GPP^{TM} LTE eight state turbo encoder. X0 and X1 are the data and interleaved data input, respectively and Y0 to Y2 are the coded outputs. Data is clocked during the low to high transition of CLK. Separate internal clock enables (CE0 and CE1) are used to clock the data into each encoder. Non–interleaved data is clocked into the first encoder and interleaved data is clocked into the second encoder. The twin vertical lines indicate a multiplexer.

The data is input in the paired sequence X_k $X_{I(k)}$ where X_k is the data at time k from 0 to K–1 and $I(k)$ is the interleaved address. The encoded data is output in parallel from the 3–bit bus Y[2:0] during each clock cycle. Table 2 shows the output sequence for each output bit. From k = 0 to K–1 the main data is encoded. The 12 tail bits are then output in the next four clock cycles, three bits at a time.

Table 2: Output sequence

Output	Sequence
Y^0	$Z^0_0 \ldots Z^0_{K-1}\ Z^0_K\ Z^1_{K+1}\ Z^2_K\ Z^3_{K+1}$
Y^1	$Z^1_0 \ldots Z^1_{K-1}\ Z^1_K\ Z^0_{K+2}\ Z^3_K\ Z^2_{K+2}$
Y^2	$Z^3_0 \ldots Z^3_{K-1}\ Z^0_{K+1}\ Z^1_{K+2}\ Z^2_{K+1}\ Z^3_{K+2}$

Note that the output is in one continuous stream. The encoder does not pause (unless YE goes low) in outputting the data.

Figure 3 shows the initial timing diagram for encoding a block of data of length K = 40. The encoder starts and ends in state 0. When the encoder requires data X0 and X1 to be read from the input RAM, the data ready signal XR goes high and X0A[12:0] and X1A[12:0] selects the non–interleaved and interleaved data bits. After a START signal is initiated XR goes high after two clock cycles. It is assumed that the data is stored in a synchronous read dual port RAM (or two single port RAMs) with XR used to control the enable input of the RAM. An asynchronous read RAM can also be used by registering the RAM output.

If YE is high, the encoded data ready signal YR goes high four clock cycles after a START signal is initiated. YR is high for both the data block and tail. If YE is low the encoder is held during the next low–to–high transition of CLK. The output of XR also goes low when YE goes low so that the data RAM output is held. Figure 4 shows the encoding process for the tail with K = 40.

The nominal input data rate f_e is

$$f_e = \frac{f_E}{1 + 7/K} \tag{1}$$

where $f_E = 1/T_{cp}$ is the encoder clock speed.

3GPP^{TM} LTE Interleaver

There are 188 standard interleaver sizes from 40 to 6144 bits. To select the internal parameters, set FS low and input the data length into K[12:0]. The encoder will automatically select the param-

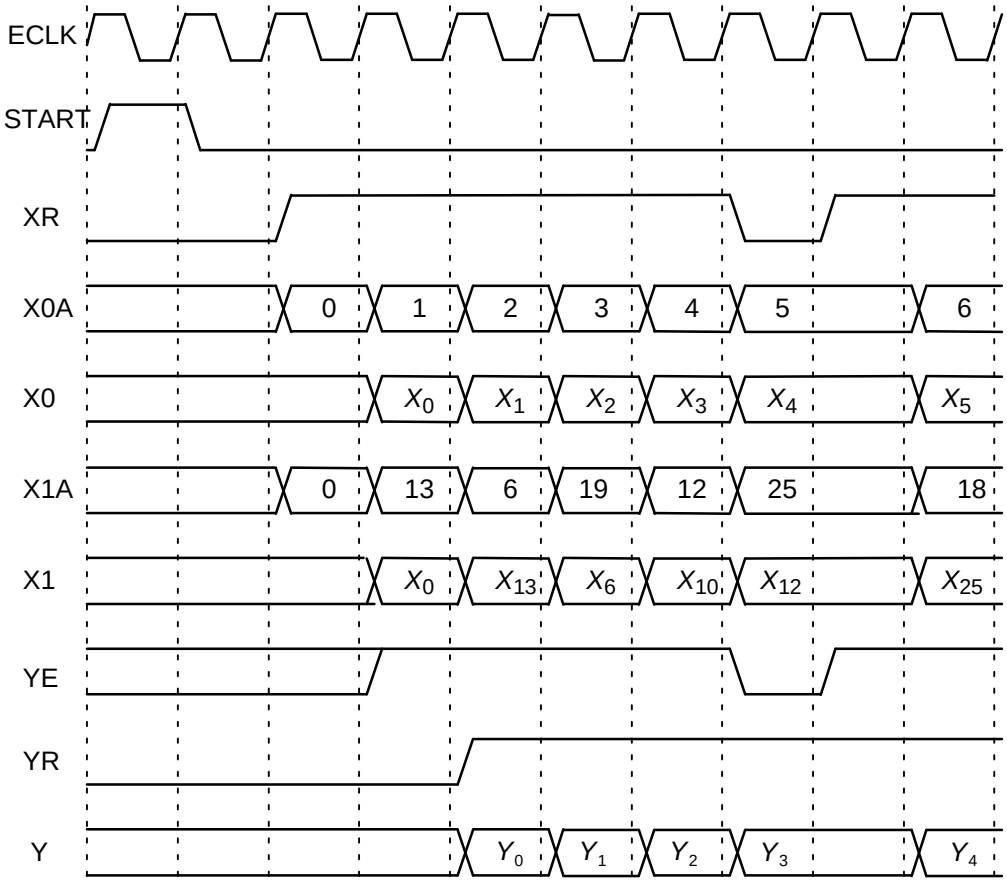

Figure 3: PCE03L Initial Encoder Timing (K = 40, R = 1/3, 3GPP™ LTE).

eters for that length. Note that the only valid lengths are from 40 to 504 bits that are a multiple of 8, 512 to 1008 bits that are a multiple of 16, 1024 to 2016 bits that are multiple of 32, and 2048 to 6144 bits that are a multiple of 64. Other interleaver lengths will cause incorrect operation.

To input external interleavber parameters, set FS high. Any length from 40 to 6144 bits can be input, provided that K is a multiple of 8. Parameter F1I[8:1] is equal to f_1 divided by two. That is, the least significant bit of f_1 is deleted since it is always equal to one due to f_1 being odd. Similarly, param-

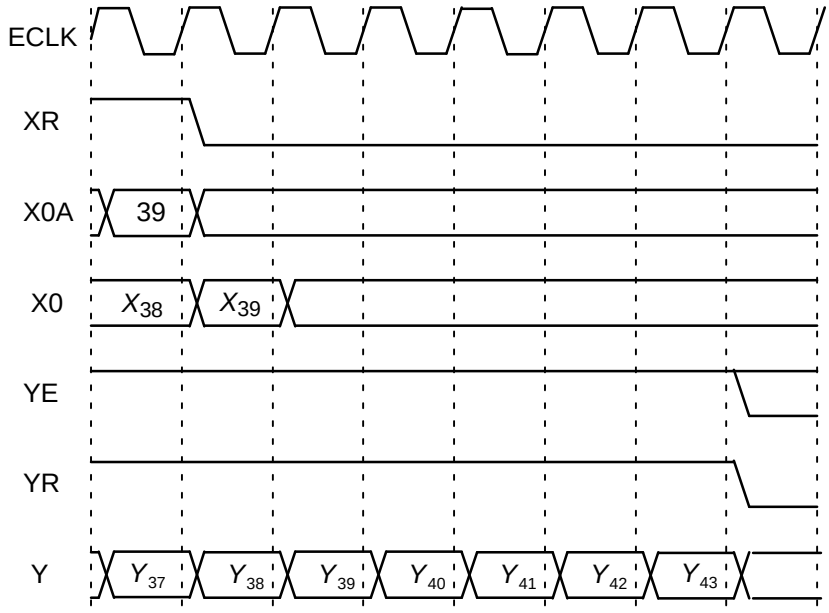

Figure 4: PCE03L Tail Encoder Timing (K = 40, R = 1/3, 3GPP™ LTE).

eter F2I[9:1] is equal to f_2 divided by two since f_2 is always even. For correct operation, $f_1 < 512$, $f_2 < 1024$, and $f_1+f_2 < 1024$.

Ordering Information

SW–PCE03L–SOS (SignOnce Site License)
SW–PCE03L–SOP (SignOnce Project License)
SW–PCE03L–VHD (VHDL ASIC License)
SW–PCE03L–UNI–n (University License)

All licenses include EDIF and VHDL cores. The VHDL cores can only be used for simulation in the SignOnce and University licenses. The University license is only available to tertiary educational institutions such as universities and colleges and is limited to n instantiations of the core. The SignOnce and ASIC licenses allows unlimited instantiations.

Note that *Small World Communications* only provides software and does not provide the actual devices themselves. Please contact *Small World Communications* for a quote.

References

[1] Third Generation Partnership Project (3GPP), "Evolved universal terrestrial radio access (E–UTRA); Multiplexing and channel coding," 3GPP TS 36.212 V8.1.0 Release 8, Nov. 2007.

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Version History

- 0.00 24 March 2009. Preliminary product specification.
- 1.00 28 April 2010. Deleted Virtex–II performance. Updated performance. Added complexity.
- 1.01 13 July 2010. Added parallel data out description.
- 1.02 13 December 2010. Updated Virtex–5 performance and complexity. Added Virtex–6 and Spartan–6 performance. Added version history.