LCE03C Features

- CCSDS TC and TM compatible
- Rate 1/2
- Data lengths of TC 64 and 256 or optional TM 1024 bits
- Up to 715 MHz internal clock
- Up to 5.5 Mbit/s encoding speed
- 76 LUTs TC or 101 LUTs and 1 18KB BlockRAM TC/TM for AMD–Xilinx Virtex–5, Spartan–6, Virtex–6, 7–Series, UltraScale and UltraScale+ FPGAs
- Available as VHDL core for AMD–Xilinx FPGAs under SignOnce IP License. Custom ASIC, Intel/Altera, Lattice and Microchip/Microsemi/Actel FPGA cores available on request.

Introduction

The LCE03C is a fully compatible CCSDS rate 1/2 telecommand (TC) (128,64), (512,256) [1] with optional telemetry (TM) (2048,1024) [2] LDPC error control encoder. Irregular quasi–cyclic LDPC codes are used. An accumulate, repeat by 4, jagged accumulate (AR4JA) LDPC code is used for the TM code. The information data length is given by *K*.

The *K* = 64 and 256 codes have circulant weights of 0, 1 or 2 with circulant sizes of 16x16 and 64x64, respectively. There are 4x8 circulants, with a check degree of 8 and a variable degree of 3 or 5 (with frequency of 1/2 each).

The *K* = 1024 code has a submatrix size of 512x512 which results in a circulant size of 128x 128. The submatrices have weights of 0, 1, 2 or 3. However, the resulting circulants have a weight of 0 or 1. There are 3x5 submatrices, with a check degree of 3 or 6 (with frequency of 1/3 and 2/3, respectively) and a variable degree of 1, 2, 3 or 6 (with frequency of 1/5, 1/5, 2/5 and 1/5, respectively). After encoding, the last 512 coded bits are punctured.

Figure 1 shows the schematic symbol for the LCE03C encoder. The VHDL core can be used with Xilinx Integrated Software Environment (ISE) or Vivado software to implement the core in Xilinx FPGA's.

Table 1 shows the performance achieved with various Xilinx parts. T_{cp} is the minimum clock period over recommended operating conditions. The encoder speed is increased by approximately 20% when only the TC codes are implemented. These performance figures may change due to device utilisation and configuration.

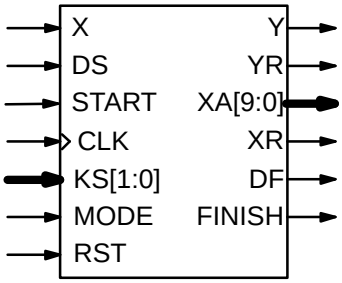

Figure 1: LCE03C schematic symbol.

Table 1: Performance of Xilinx parts.

Xilinx Part	T_{cp} (ns)	f_e (Mbit/s)
XC7S6C–1	4.100	1.90
XC7S6C–2	3.397	2.29
XC7A12T–1	4.043	1.93
XC7A12T–2	3.413	2.28
XC7A12T–3	2.989	2.61
XC7K70T–1	3.160	2.47
XC7K70T–2	2.707	2.88
XC7K70T–3	2.405	3.24
XCKU035–1	2.700	2.89
XCKU035–2	2.352	3.32
XCKU035–3	1.920	4.06
XCKU3P–1	1.730	4.51
XCKU3P–2	1.552	5.03
XCKU3P–3	1.398	5.58

Signal Descriptions

CLK System Clock
FINISH Encoder Finish
KS Data Length Select
0 = 64
1 = 256
2 = 1024
MODE Maximum Data Length Select
0 = 64 or 256
1 = 64, 256 or 1024
RST Synchronous Reset

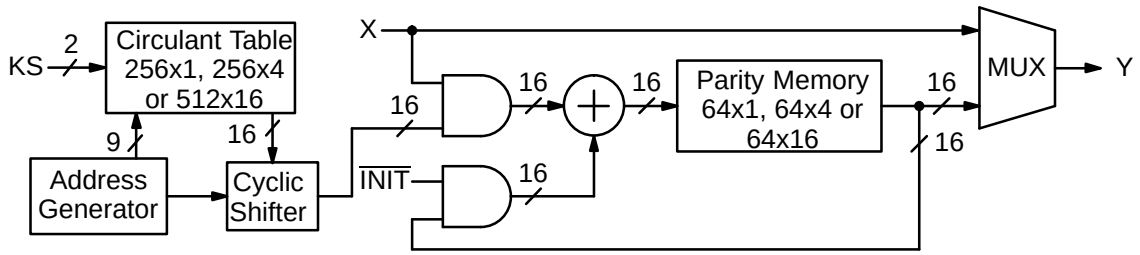

Figure 2: LCE03C Systematic Encoder.

START Encoder Start
X Data In
XA Data In Address
XR Data In Ready
DF Data Finish
DS Data Start
Y Data Out
YR Data Out Ready

The MODE input is used to select the device configuration. It is a “soft” input and should not be connected to input pins or logic.

Encoder

Figure 2 gives a block diagram of the LCE03C encoder. X is the data input and Y is the coded output. Data is clocked during the low to high transition of CLK. The Cyclic Shifter is only used for K = 1024.

The data is input one bit at a time in the sequence X_k from time k = 0 to K–1, where K = 64, 256 or 1024. While data is entered, the output Y selects the input data X. After the data is input, the output Y selects the parity memory for K output bits. During the first 64 clock cycles, the signal $\overline{\text{INIT}}$ is low so as to initialise the Parity Memory.

Figure 3 shows the initial timing diagram. The data start input DS must go high for one clock cycle for each bit to be output. To start the encoder START should go high for one clock cycle. The first DS can go high during START or later. The first data bit X_0 is then synchronously read from an external input memory using XA as the read address. Two clock cycles after DS goes high, the first coded bit Y_0 is output, which is equal to X_0. The output YR also goes high for one clock cycle. The earliest that the next DS can go high is when DF goes high. DS can go high at the same time as DF, or later if desired.

DS going high starts the internal parity calculation for the data bit being input. After 64 clock cycles DF goes high. If START + DF (where + indicatates logical OR) is input to DS, the encoder will automatically encode the rest of the block. The read enable to the input memory should be START + XR.DS where . indicates logical AND.

Alternatively, DS can be used to asynchronously control the encoding process, as long as minimum time between DS going high is 64 clock cycles.

Figure 4 shows the encoding process at the start of the parity data being output. After the last data bit has been input XR will go low. Figure 5 shows the timing for the last coded bits being output. The signal FINISH going high indicates the end of the encoding process. If desired, START and DS can go high at the same time as FINISH goes high (or later if desired) to start the next encoded block.

The nominal average input data rate f_e is

$$f_e = \frac{f_E}{128} \tag{1}$$

where $f_E = 1/T_{cp}$ is the encoder clock speed. The coded rate is $2f_e$.

Ordering Information

SW–LCE03C–SOS (SignOnce Site License)
SW–LCE03C–SOP (SignOnce Project License)
SW–LCE03C–VHD (VHDL ASIC License)

All licenses include Xilinx VHDL cores. The SignOnce and ASIC licenses allows unlimited instantiations.

Note that *Small World Communications* only provides software and does not provide the actual devices themselves. Please contact *Small World Communications* for a quote.

References

[1] Consultative Committee for Space Data Systems, “Recommendation for space data system standards: TC synchronization and channel coding,” CCSDS 231.0–B–3, Blue Book, Sep. 2017.

[2] Consultative Committee for Space Data Systems, “Recommendation for space data system standards: TM Synchronization and channel coding,” CCSDS 131.0–B–3, Blue Book, Sep. 2017.

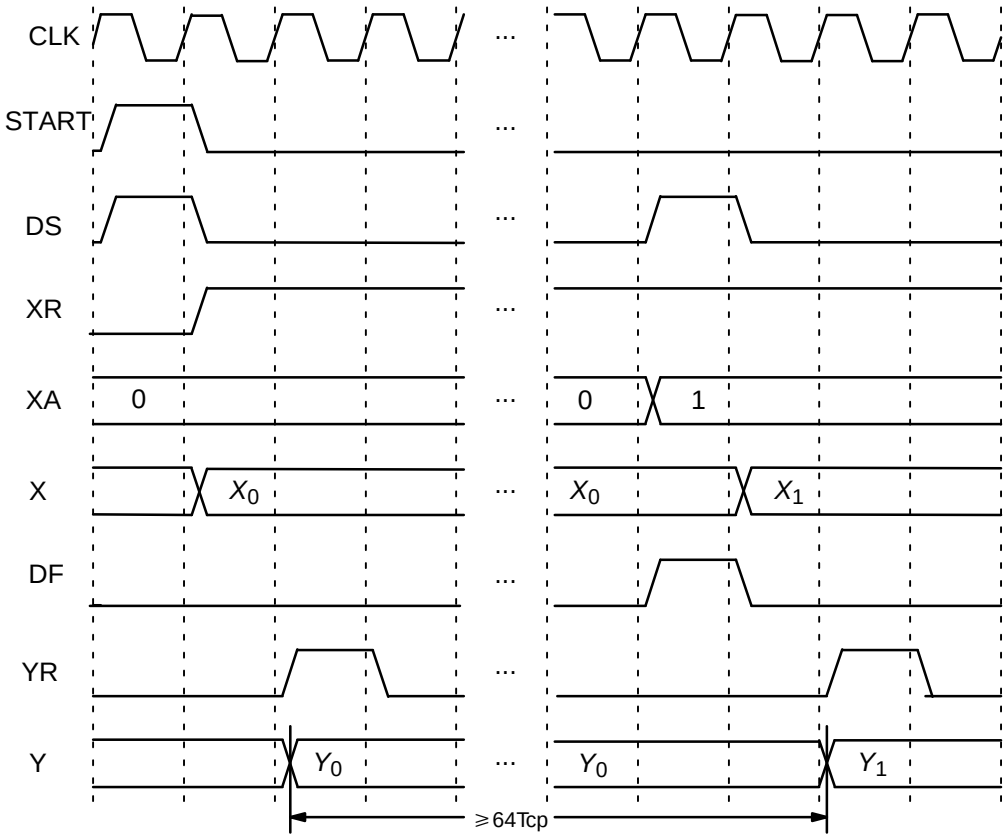

Figure 3: LCE03C initial encoder timing.

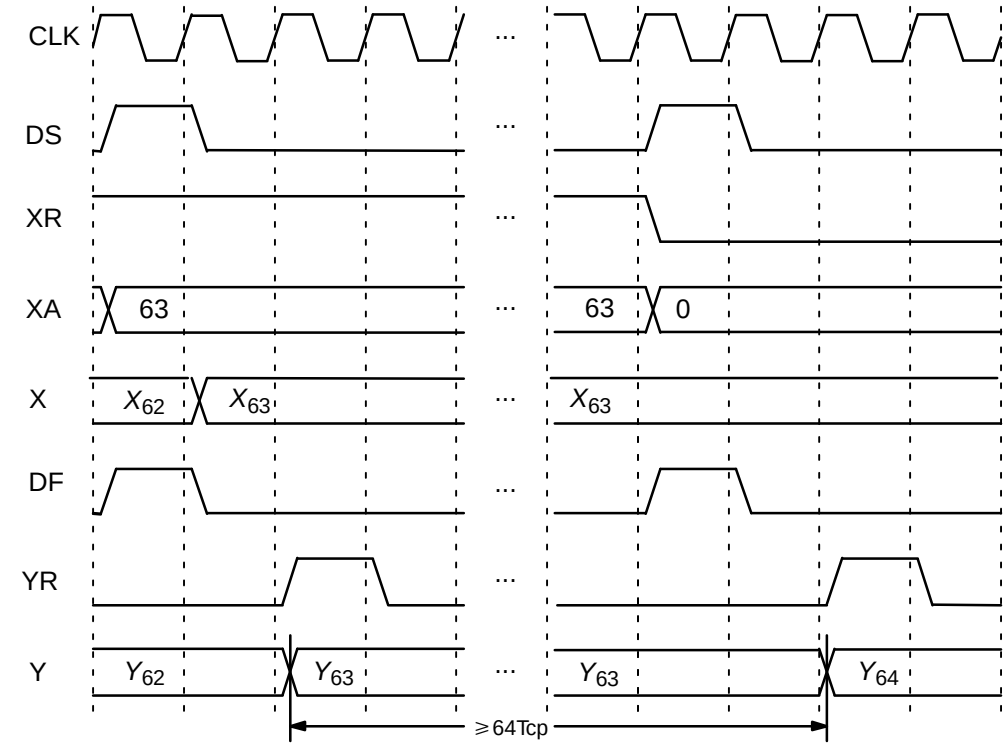

Figure 4: LCE03C encoder start of parity timing (K = 64).

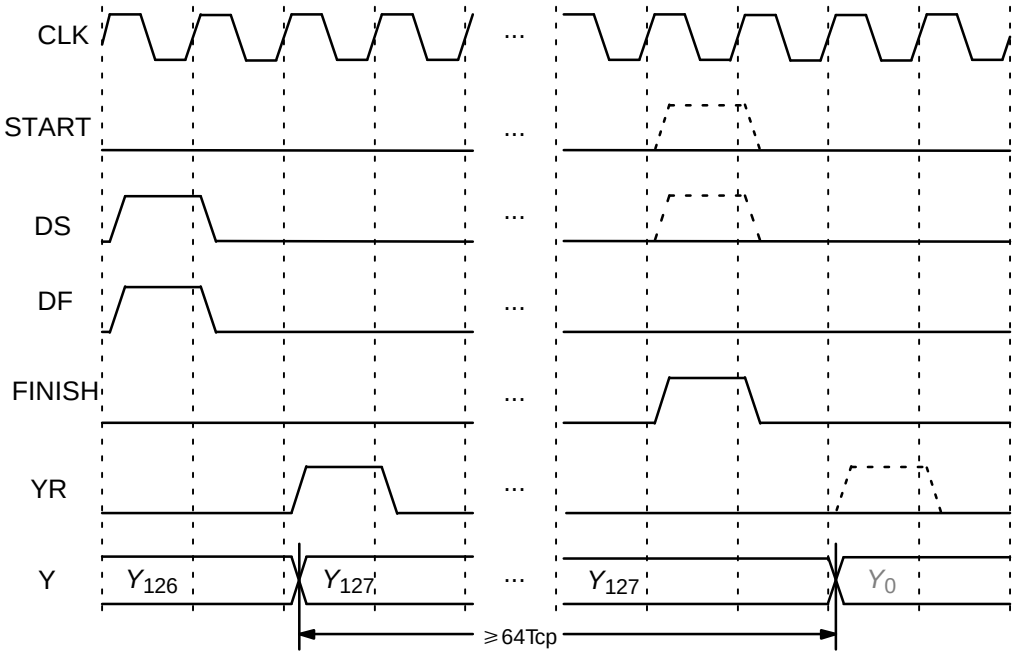

Figure 5: LCE03C encoder end of parity timing (K = 64).

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Revision History

- v0.00 17 Nov. 2021. Preliminary product specification.
- v0.01 19 Nov. 2021. Changed XYS and XYF to DS and DF. Corrected timing.
- v0.02 26 Nov 2021. Added performance and complexity for MODE = 0.
- v1.00 21 Mar. 2022. First release. Corrected Figure 2. Added performance and complexity for MODE = 1.
- v1.01 10 May 2022. Updated LUT complexity.