LCE02C Features

- CCSDS TM AR4JA compatible
- Rate 1/2, 2/3 and 4/5
- Data lengths of 1024 or 4096 bits
- Up to 605 MHz internal clock
- Up to 60 Mbit/s encoding speed
- 1090 LUTs and 15 18KB BlockRAMs for AMD–Xilinx Virtex–5, Spartan–6, Virtex–6, 7–Series, UltraScale and UltraScale+ FPGAs
- Available as VHDL core for AMD–Xilinx FPGAs under SignOnce IP License. Custom ASIC, Intel/Altera, Lattice and Microchip/Microsemi/Actel FPGA cores available on request.

Introduction

The LCE02C is a compatible CCSDS rate R = 1/2, 2/3 and 4/5 telemetry (TM) [1] LDPC error control encoder. Data lengths of 1024 and 4096 are supported. Irregular quasi–cyclic LDPC codes are used. An accumulate, repeat by four, jagged accumulate (AR4JA) LDPC code is used. The information data length is given by K and the number of coded bits by N.

The rate 1/2 codes have a submatrix size M of 512 or 2048 which results in a circulant size M_c of 128 or 512. The submatrices have weights of 0, 1, 2 or 3. However, the resulting circulants have a weight of 0 or 1. There are 3x5 submatrices, with a check degree of 3 or 6 (with frequency of 1/3 and 2/3, respectively) and a variable degree (d_v) of 1, 2, 3 or 6 (with frequency of 1/5, 1/5, 2/5 and 1/5, respectively). After encoding, the last 512 or 2048 coded bits are punctured. The number of submatrix rows q is 3 for all codes.

The rate 2/3 and 4/5 codes have a similar structure, with 3x7 and 3x11 submatrices, respectively. The last M coded bits are also punctured. Tables 1 and 3 gives the parameters for all the codes. The average check and variable degrees are given by d_c and d_v, respectively.

Figure 1 shows the schematic symbol for the LCE02C encoder. The VHDL core can be used with Xilinx Integrated Software Environment (ISE) or Vivado software to implement the core in Xilinx FPGA's.

Table 2 shows the performance achieved with various Xilinx parts. T_{cp} is the minimum clock period over recommended operating conditions. These performance figures may change due to device utilisation and configuration.

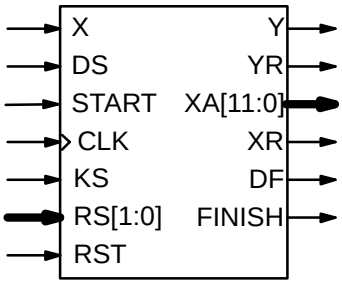

Figure 1: LCE02C schematic symbol.

Table 1: LDPC Code Parameters (bit lengths)

Rate	K	N	M	M_c	Mqd_c
1/2	1024	2048	512	128	7680
2/3	1024	1536	256	64	5888
4/5	1024	1280	128	32	4992
1/2	4096	8192	2048	512	30720
2/3	4096	6144	1024	256	23552
4/5	4096	5120	512	128	19968

Table 2: Performance of Xilinx parts.

Xilinx Part	T_{cp} (ns)	f_e (Mbit/s)		
		R = 1/2	R = 2/3	R = 4/5
XC7S15C–1	4.332	14.42	19.23	23.08
XC7S15C–2	3.626	17.23	22.98	27.57
XC7A12T–1	4.416	14.15	18.87	22.64
XC7A12T–2	3.654	17.10	22.80	27.36
XC7A12T–3	3.193	19.57	26.09	31.31
XC7K70T–1	3.330	18.76	25.02	30.03
XC7K70T–2	2.828	22.10	29.46	35.36
XC7K70T–3	2.523	24.77	33.02	39.63
XCKU035–1	2.860	21.85	29.13	34.96
XCKU035–2	2.492	25.08	33.44	40.12
XCKU035–3	2.054	30.42	40.57	48.68
XCKU3P–1	2.052	30.45	40.61	48.73
XCKU3P–2	1.847	33.83	45.11	54.14
XCKU3P–3	1.651	37.85	50.47	60.56

Table 3: LDPC Code Parameters (check and variable degrees)

Rate	$d_{c,\text{range}}$	$d_{c,\text{freq}}$	d_c	$d_{v,\text{range}}$	$d_{v,\text{freq}}$	d_v	qd_c
1/2	3,6	(1,2)/3	5	1,2,3,6	(1,1,2,1)/5	3	15
2/3	3,10	(1,2)/3	7.667	1,2,3,4,6	(1,1,2,2,1)/7	3.286	23
4/5	3,18	(1,2)/3	13	1,2,3,4,6	(1,1,2,6,1)/11	3.545	39

Signal Descriptions

CLK System Clock
FINISH Encoder Finish
KS Data Length Select
0 = 1024
1 = 4096
RS Code Rate Select
0 = 1/2
1 = 2/3
2 = 4/5
RST Synchronous Reset
START Encoder Start
X Data In
XA Data In Address
XR Data In Ready
DF Data Finish
DS Data Start
Y Data Out
YR Data Out Ready

Encoder

Figure 2 gives a block diagram of the LCE02C encoder. X is the data input and Y is the coded output. Data is clocked during the low to high transition of CLK.

The data is input one bit at a time in the sequence X_k from time $k = 0$ to $K–1$, where $K = 1024$ or 4096. While data is entered, the output Y selects the input data X. After the data is input, the output Y selects the parity memory for $N–K$ output bits. One data bit is entered every eight clock cycles. During the first eight clock cycles, the signal $\overline{\text{INIT}}$ is low so as to initialise the Parity Memory.

The Rotate Left operation depends on the circulant size M_c. For M_c = 512, 256, 128, 64 and 32, one 512–bit, two 256–bit, four 128–bit, eight 64–bit or eight 32–bit rotate lefts are chosen, respectively. After the data bits are input signal XE goes low and the Rotate Left circuit is used to output the parity bits from the Parity Memory. Due to the intial rotations, the second least significant bit of the corresponding Parity Memory output is selected.

Figure 3 shows the initial timing diagram. The data start input DS must go high for one clock cycle for each bit to be output. To start the encoder START should go high for one clock cycle. The first DS can go high during START or later. The first data bit X_0 is then synchronously read from an external input memory using XA as the read address. Two clock cycles after DS goes high, the first coded bit Y_0 is output, which is equal to X_0. The output YR also goes high for one clock cycle. The earliest that the next DS can go high is when DF goes high. DS can go high at the same time as DF, or later if desired.

DS going high starts the internal parity calculation for the data bit being input. After eight clock cycles DF goes high. If START + DF (where + indicatates logical OR) is input to DS, the encoder will automatically encode the rest of the block. The read enable to the input memory should be START + XR.DS where . indicates logical AND.

Alternatively, DS can be used to asynchronously control the encoding process, as long as minimum time between DS going high is eight clock cycles.

Figure 4 shows the encoding process at the start of the parity data being output. After the last data bit has been input XR will go low. Figure 5 shows the timing for the last coded bits being output. The signal FINISH going high indicates the

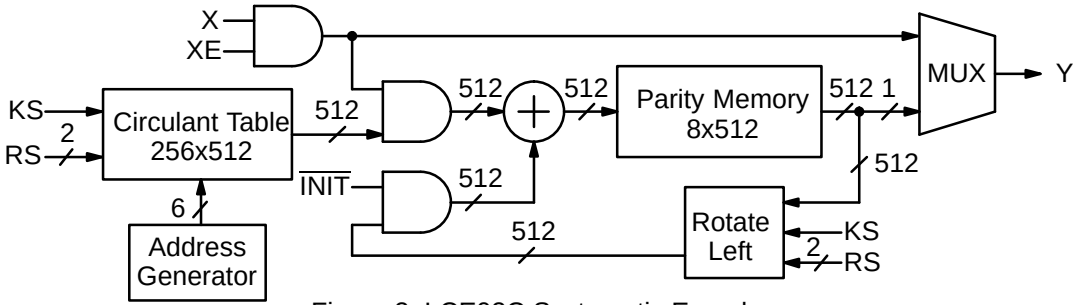

Figure 2: LCE02C Systematic Encoder.

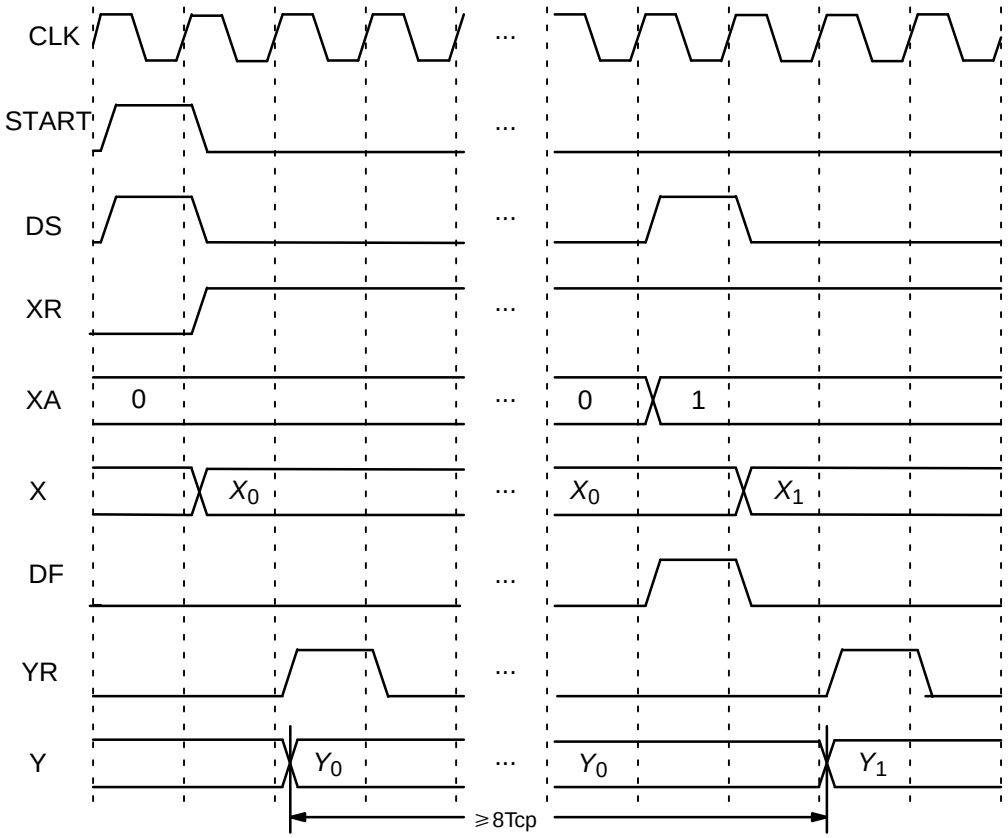

Figure 3: LCE02C initial encoder timing.

end of the encoding process. If desired, START and DS can go high at the same time as FINISH goes high (or later if desired) to start the next encoded block.

The nominal average input data rate f_e is

$$f_e = \frac{f_E R}{8} \quad (1)$$

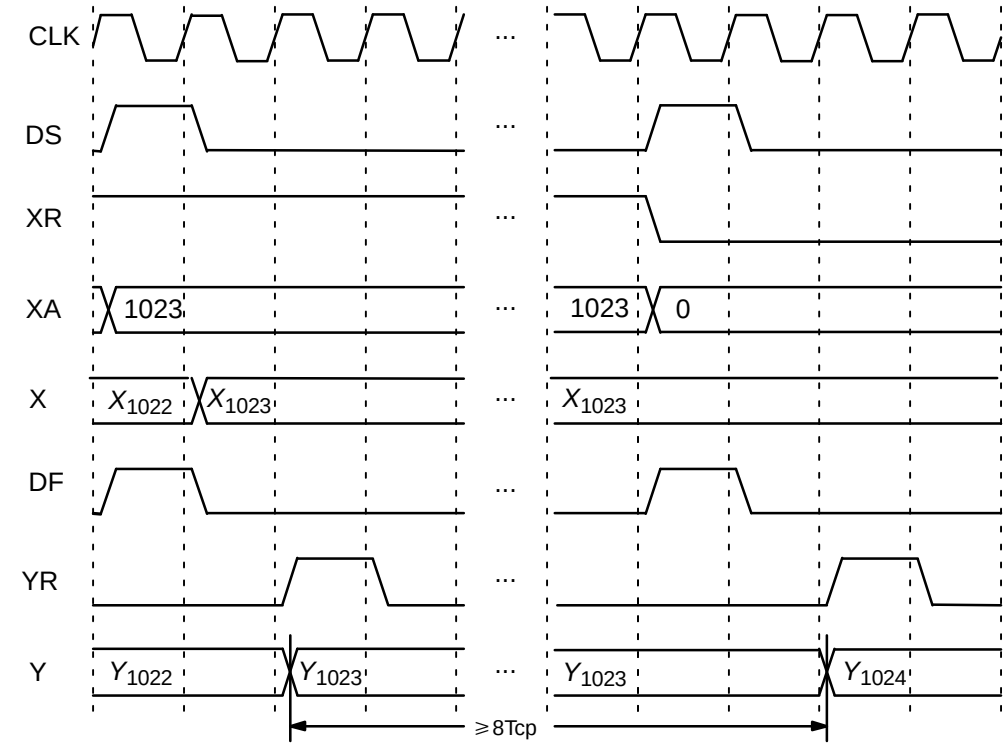

Figure 4: LCE02C encoder start of parity timing (K = 1024).

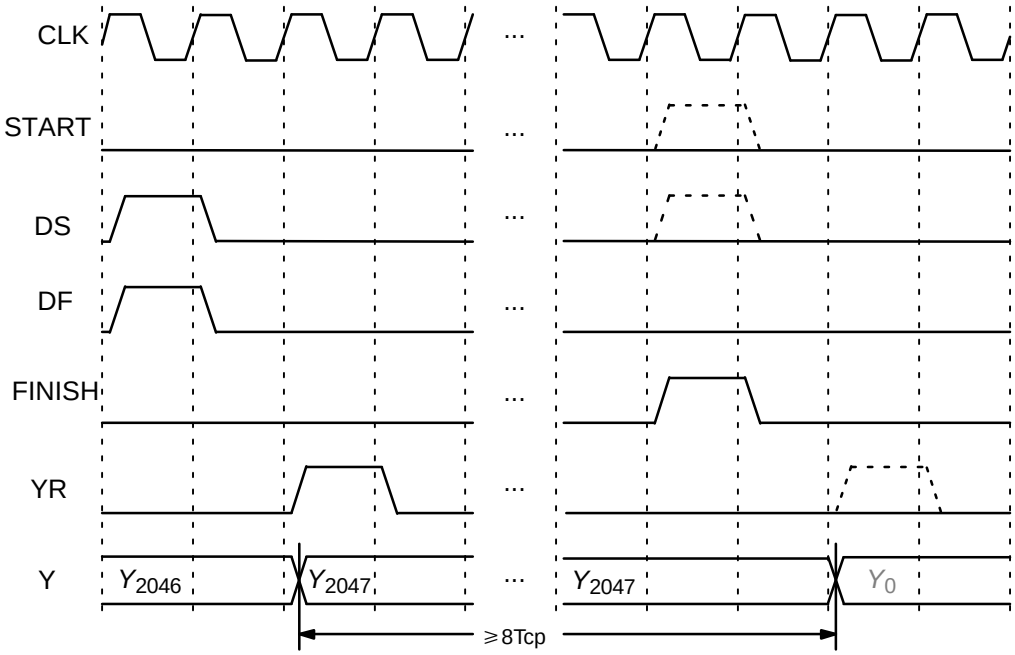

Figure 5: LCE02C encoder end of parity timing (K = 1024, R = 1/2).

where $f_E = 1/T_{cp}$ is the encoder clock speed. The coded rate is $f_E/8$.

Ordering Information

SW–LCE02C–SOS (SignOnce Site License)
SW–LCE02C–SOP (SignOnce Project License)
SW–LCE02C–VHD (VHDL ASIC License)

All licenses include Xilinx VHDL cores. The SignOnce and ASIC licenses allows unlimited instantiations.

Note that *Small World Communications* only provides software and does not provide the actual devices themselves. Please contact *Small World Communications* for a quote.

References

[1] Consultative Committee for Space Data Systems, “Recommendation for space data system standards: TM Synchronization and channel coding,” CCSDS 131.0–B–3, Blue Book, Sep. 2017.

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Revision History

- v0.00 22 Apr. 2022. Preliminary product specification.
- v1.00 20 May 2022. First release. Added implementation complexity and performance.