LCE01C Features

- CCSDS compatible
- Rate 223/255 (8160,7136)
- Up to 600 MHz internal clock
- Up to 4.18 Gbit/s input data rate
- 8–bit byte input and output
- 9,209 6–input LUTS. 10,200 Altera ALUTs.
- Asynchronous logic free design
- Available as EDIF and VHDL core for Xilinx FPGAs under SignOnce IP License. ASIC, Intel/Altera, Lattice and Microsemi/Actel cores available on request.

Introduction

The LCE01C is a fully compatible CCSDS rate 223/255 (8160,7136) LDPC [1] error control encoder. A regular quasic–cyclic LDPC code with 511x511 square circulants with weight 2 in the parity check matrix is used. There are 2x16 circulants, resulting in a check node degree of 32 and a variable node degree of 4.

Figure 1 shows the schematic symbol for the LCE01C encoder. The EDIF core can be used with Xilinx Foundation or Integrated Software Environment (ISE) software. The VHDL core can be used with Xilinx ISE or Vivado software. Custom VHDL cores can be used in ASIC designs.

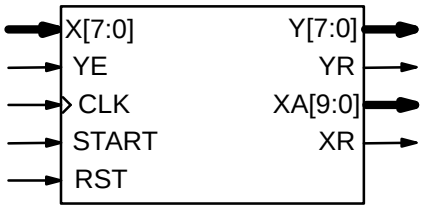

Figure 1: LCE01C schematic symbol.

Table 1 shows the performance achieved with various Xilinx parts. T_{cp} is the minimum clock period over recommended operating conditions. These performance figures may change due to device utilisation and configuration. Note that Zynq devices up to XC7Z020 and from XC7Z030 use programmable logic equivalent to Artix–7 and Kintex–7 devices, respectively.

Table 1: Performance of Xilinx parts.

Xilinx Part	T_{cp} (ns)	Mbit/s
XC7S50–1	5.139	1357
XC7S50–2	4.200	1660
XC7A50T–1	4.940	1412
XC7A50T–2	4.065	1716
XC7A50T–3	3.598	1938
XC7K70T–1	3.346	2084
XC7K70T–2	2.707	2576
XC7K70T–3	2.445	2852
XCKU035–1	2.716	2568
XCKU035–2	2.302	3030
XCKU035–3	2.043	3414
XCKU3P–1	2.076	3360
XCKU3P–2	1.805	3864
XCKU3P–3	1.665	4189

Signal Descriptions

CLK System Clock
RST Synchronous Reset
START Encoder Start
X Data In
XA Data In Address
XR Data In Ready
Y Data Out
YE Data Out Enable
YR Data Out Ready

Encoder

Figure 2 gives a block diagram of the LCD01C encoder. X is the data input and Y is the coded output. Data is clocked during the low to high transition of CLK.

The data is input eight bits at a time in the sequence $X_k = \{x_{8k},...,x_{8k+7}\}$ from time $k = 0$ to $K/8–1$, where $K = 7136$. That is, the first bit of the first data symbol X[7:0] to be encoded is the most significant bit X[7]. Similarly, the first bit of the first encoded symbol Y[7:0] to be transmitted is the most significant bit Y[7].

As 8 is not a factor of the circulant size of 511, this implies that two circulant tables are required. One circulant table is used when all eight inputs

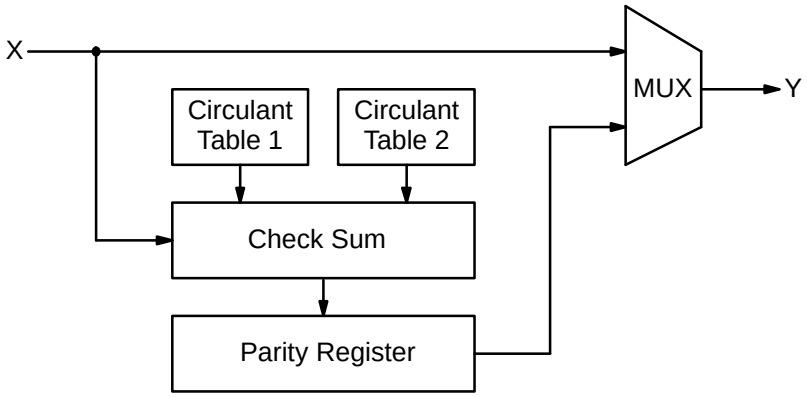

Figure 2: LCE01C Systematic Encoder.

select rows within one circulant. Two tables are used when the eight inputs stradle two circulants.

While data is entered, the output Y selects the input data X. After the data is input, the output Y selects the parity register for $(N–K)/8 = 128$ clock cycles.

Note that the output is one continuous stream. The encoder does not pause (unless YE goes low) in outputting the data. If YE goes low, then the input data must be held.

Figure 3 shows the initial timing diagram. When the encoder requires data X to be read from the input RAM, the data ready signal XR goes high and XA[9:0] selects the data byte. After a START signal is initiated XR goes high after one cycle. It is assumed that the data is stored in a synchronous read RAM. The signals XR and YE can be used to control the enable input of the RAM. An asynchronous read RAM can also be used by registering the RAM output. Input data X only needs to be valid when YE is high.

If YE is high, the encoded data ready signal YR goes high three clock cycles after a START signal is initiated. YR is high for both the data block and parity. If YE is low the encoder is held during the next low–to–high transition of CLK.. Figure 4 shows the encoding process for the parity. It is assumed that the first transmitted bit is $Y_0[7]$.

The nominal input data rate f_e is

$$f_e = \frac{f_E K}{N/8 + 3} \tag{1}$$

where $f_E = 1/T_{cp}$ is the encoder clock speed. For the (8160,7136) code, this results in $f_e = 6.9755 f_E$.

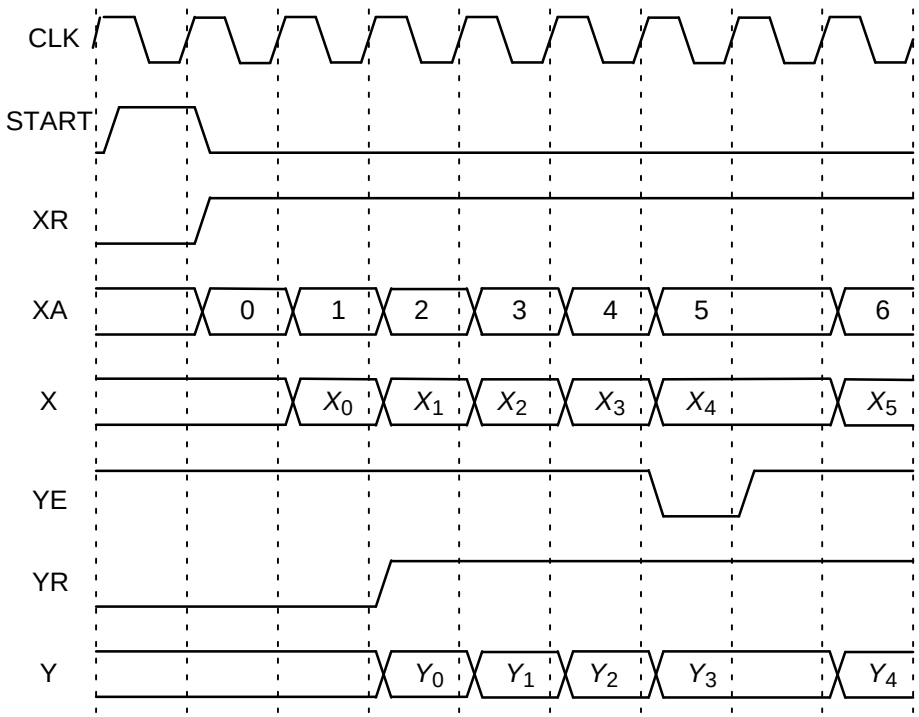

Figure 3: LCE01C Initial Encoder Timing.

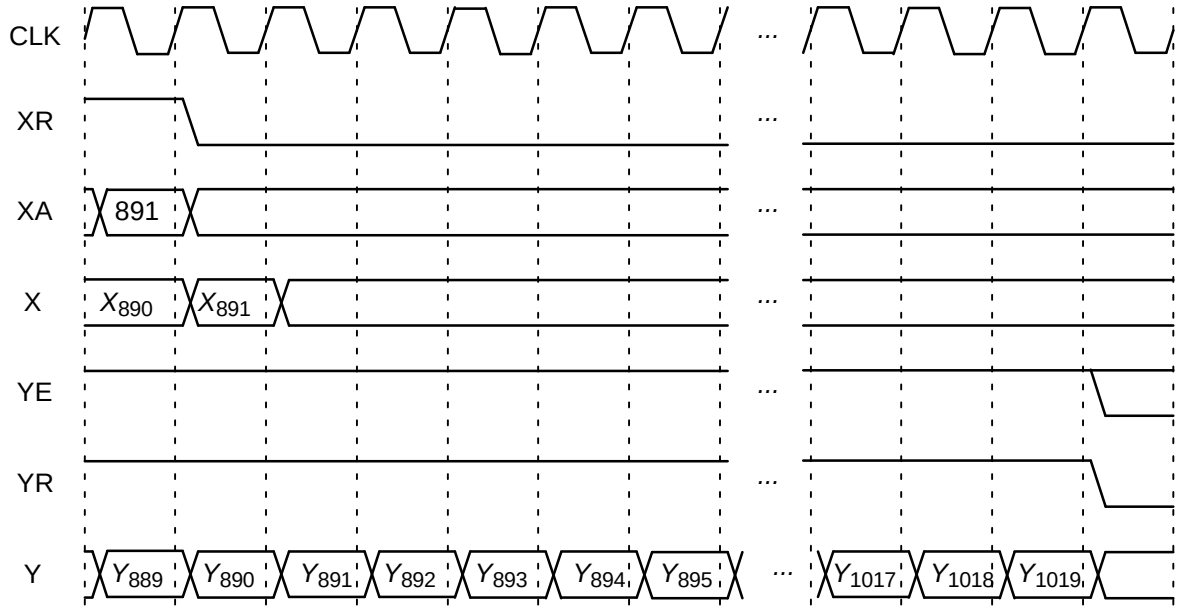

Figure 4: LCE01C encoder parity timing.

Ordering Information

SW–LCE01C–SOS (SignOnce Site License)
SW–LCE01C–SOP (SignOnce Project License)
SW–LCE01C–VHD (VHDL ASIC License)

All licenses include EDIF and VHDL cores. The SignOnce and ASIC licenses allows unlimited instantiations. The EDIF core can be used for Virtex–2, Spartan–3 and Virtex–4 with Foundation or ISE software. The VHDL core can be used for Virtex–5, Spartan–6, Virtex–6, 7–Series, UltraScale and UltraScale+ with ISE or Vivado software.

Note that *Small World Communications* only provides software and does not provide the actual devices themselves. Please contact *Small World Communications* for a quote.

References

[1] Consultative Committee for Space Data Systems, “TM synchronization and channel coding,” CCSDS 131.0–B–2, Aug. 2011.

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Revision History

- v0.00 20 Aug. 2012. Preliminary product specification.
- v1.00 27 Mar. 2013. Added Xilinx performance and complexity.
- v1.01 8 Aug. 2023. Deleted Spartan–3, Virtex–4, Virtex–5, Spartan–6 and Virtex–6 performance. Updated Artix–7 and Kintex–7 performance and complexity. Added Spartan–7, UltraScale and UltraScale+ performance.